

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	trap adj handl\$3 near5 hint adj code	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/01/06 15:03
L2	0	trap adj handl\$3 near5 hint	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/01/06 15:03
L3	67	trap adj handl\$3 near5 branch	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/01/06 15:06
L4	70	trap adj handl\$3 near5 (branch or prefetch or pre adj fetch)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/01/06 15:14
L5	3	4 not 3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/01/06 15:06
L6	72	(trap or interrupt) adj handl\$3 near10 (prefetch or pre adj fetch)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/01/06 15:10
L7	63	(trap or interrupt) adj handl\$3 near5 (prefetch or pre adj fetch)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/01/06 15:09
L8	10	(trap or interrupt) adj handl\$3 adj10 (prefetch or pre adj fetch)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/01/06 15:13
L11	30	(trap or interrupt) adj handl\$3 near5 (branch or prefetch or pre adj fetch) and break	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/01/06 15:15

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(trap OR interrupt) handler "prefetch hint" file

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**handler** needs to branch directly to the appropriate **trap handler** instead of performing

... Section 4.5.1, just before Table 4-51 "Sequential **Prefetch Hint** ...

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counter value is set up to **interrupt** the processor after a pre-determined number of events have been ... data **prefetch hint** 1:140. loads from memory 1:139 ...

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This provides a **prefetch hint** to the processor, allowing the ... **trap handler** that will then branch to the recovery code. Improving the fault recovery on ...

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**Interrupt** vector 19 used to invoke unmasked exception. handlers. handlers. —

Provide larger (512 bytes of state) context record to **handler** ...

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arithmetic **trap handler** is required. The **trap** barrier checks the ... but this

post-increment can also be used to give a **prefetch hint** for the start address ...

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ports **prefetch hint** calls that allow a user-level execution to specify ... the appropriate signal **handler** (the function previously designated as the ...

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Set Reference. Revision 2.0. December 2001. Document Number: 245319-003 ...

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Otherwise, the Illegal Word Access **trap** will. be invoked when this channel is used.

5.4.3. PEC **Handler Interrupt** Actions Summary ...

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In addition, IA-64 enables low latency fault, **trap**, and **interrupt** ... Note that the software exception **handler** could examine the Flush-to-Zero mode bit and ...  
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as a fault where the fault-**handler** emulates the branch. Although the expected mode of ... A **prefetch hint** is implied in the base update forms. The address ...  
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immediately at the end of the excepting instruction. The **handler** is invoked. through the Streaming SIMD Extensions exception **interrupt** (vector 19), ...  
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latency fault, **trap**, and **interrupt** handlers along with light-weight domain crossings. ... Note that the software exception **handler** could examine the ...  
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causes any Itanium traps (e.g., Single Step **trap**, Taken Branch **trap**, or ... A **prefetch hint** is implied in the base update forms. The ...  
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branch **prefetch hint**. • t bhint d bhint. branch direction hint. • t chint d chint ... true if the **interrupt** is a **trap**. • bool isexec (void) const ...  
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In addition, IA-64 enables low latency fault, **trap**, and **interrupt** handlers along ... Sequential **Prefetch Hint** on Branches. Completer. Sequential Prefetch ...  
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with a focus on how external asynchronous **interrupt** handling can be controlled by software. ... A **prefetch hint** is implied in the base update forms. The ...  
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Instruction Address **trap**), IIP will contain the original 64-bit target IP. ... A **prefetch hint** is implied in the base update forms. The ...  
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Software prefetching requires a programmer to use **PREFETCH hint** instructions and

... and **trap** for an exception if one occurs. Catching the exception in a ...  
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Immediately at the end of the excepting instruction. The **handler** is invoked. t. " hrough  
the Streaming SIMD Extensions exception **interrupt** (vector 19), ...

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**Hints** for performance optimizations when using the. MPC8xx family: ... For the case of a frequently activated **interrupt handler**, consider locking in (if the ...

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wait the 250  $\mu$ s A/D conversion delay from within the OC5 **handler**. You may NOT have any. backwards jumps in the **interrupt handler**. (**Hint**, there is an answer ...

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**interrupt handler(s)** will measure the pulse widths in the waveform. ...

**Hints/clarifications.** 1) You can write the software that measures pulse width, ...

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ecutes the **interrupt handler** in the same address space. What should the system do?

... mer **hints** for conflict resolution. For instance, an argu- ...

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Since a round trip through the system **interrupt handler** and the driver's **interrupt** ...

So some **hints** for optimizing performance are: ...

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Debugging **Hints** for Writing a Bus Error **Handler** for the '040 ... error happened during execution of an **interrupt handler** or noninterrupt-level code. ...

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Given proper **hints**, identifies. application blocks. . Task. . **Interrupt handler**. . OS

routine. . Maps blocks to RTG program ...

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At least 1 pushbutton (PB) **interrupt handler** activating. on a falling-edge transition ...

Optionally executes a **TRAP 0** to attempt to restart the ...

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**[PDF] Section I: Lab 2 Tutorial Notes**

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Timer 1 **interrupt handler** performs the following steps: ... **Hints** for Lab 2. • Use the same names for your peripherals and signals as you did ...

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Interrupts: **interrupt handler** can't afford to wait to acquire a monitor lock. ... Inktomi uses **hints** for fault tolerance: if the **hint** is wrong, things we'll ...

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**[PDF] Appendix C Data Acquisition and Control—Some Hints**

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ize the **interrupt** vector to point to the proper **interrupt handler**. ... Section C.2 gives some **hints** for one method of interfacing Turbo C code to an ...

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to take one inside an **interrupt** service routine? Why might it be a good idea to move a task into an **interrupt handler**? (**Hint**: Think ...

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Is it possible for a **handler** to distinguish between a **trap**, a fault, an abort, and an **interrupt**? If yes, describe how. If no, why not? ...

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(b) the **interrupt** vector is used to index into a table to retrieve the **interrupt handler's** address. (c) the hardware actions upon a **trap** and **interrupt** are ...

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(n) When an **interrupt** arrives, the task of looking up the table of **interrupt handler** addresses ... [**Hint**: Access shared variables in critical sections only! ...

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**handler**. After control is passed to. **trap()**. , that function handles the exception/**interrupt** or. dispatches the exception/**interrupt** to a specific **handler** ...

[ocw.mit.edu/.../6-828Fall2003/](http://ocw.mit.edu/.../6-828Fall2003/)

[47DE1D8E-942E-4A58-9FE9-B40C7B076824/0/lab3.pdf](http://47DE1D8E-942E-4A58-9FE9-B40C7B076824/0/lab3.pdf) - [Similar pages](#)

**[PDF] Pipelined Beta**

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E. Access to XP by the first instruction in an **interrupt handler**. ... **Hint:** consider how long it would take the original pipelined ...

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unused slots in the ROB, we in-line the **interrupt handler** code ... the application-for example, the TLB contents are merely a **hint** ...

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**hint** telling which is the node caching the most recent block ... which serves the blocks using a software **interrupt handler**. run in interruptible context. ...

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**[PDF] 6.004 Fall 1997 - 1 - Problem Set #7 M A S S A C H U S E T T S ...**

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**Hint:** there are four bugs having to do with missing components and ... address of the **interrupt handler**, XAdr, is loaded into the PC at the end of cycle I ...

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**[PDF] 6.004 Spring 2000 - 1 - Problem Set #8 M A S S A C H U S E T T S ...**

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**Hint:** consider how long. it would take the original pipelined Beta to complete a sequence of ... first lines of the **interrupt handler**: XAdr: ADDC(SP,4,SP) ...

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**[PDF] There have been several questions regarding lab 5, and I have ...**

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**Hint:** read the section in the lab report that discusses the IMMR ... you return from your **interrupt handler** or these interrupts will be permanently ...

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**[PDF] EECS 373 Fall 1998 Lab 5: Timers & Multiple Interrupts**

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Notes and **hints**: 1. The main code for your **interrupt handler** should take care of the register sav-. ing, and then use if-then type statements to determine ...

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own code as a **trap handler**. Then, you can simply cause a **trap** to happen, ...

Assuming that the ACIA is set up, write the **interrupt handler** for receive: ...

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**Hint:** the table on page 1 might prove useful. Instruction. Next PC (32-bit) ... Assuming that the ACIA is set up, write the **interrupt handler** for receive: ...

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[PDF] [Improving the Precise Interrupt Mechanism of Software- Managed TLB ...](#)

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This paper presents a novel method of in-lining the **interrupt handler** ... to the application—for example, the TLB contents are merely a **hint** for better ...

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The NBP name for both an agent and a **trap handler** should be stable - ... a **hint** to perform an NBP confirm (which sends a unicast to the ...

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...

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**interrupt handler** is usually extremely primitive compared to the ... worth asking TCP to cache a **hint** for each connection, which can be ...

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time, accurately measuring **interrupt handler** performance. is difficult with the traditional ... that gives a **hint** to the operating system about where to ...

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At the same time, accurately measuring **interrupt handler** per- ... a tool that gives a **hint** to the operating system about where to create superpages (which ...

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receive an **interrupt**? (**Hint**: The VMM relies on the host for actual device driver support.) ... system's TSS and jump the host OS's **trap handler**. ...

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**Hint**: you could mention the role. of ROM memory, how the operating system is loaded, ... **interrupt handler** and kernel (context switching) runs for 200 ...

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**Hint**: there. is probably an error in this command, yet something will happen. ...

**interrupt handler** and kernel (context switching) runs for 200 instructions ...

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Maybe **hints** for other operating systems ... Resource management. 5. PCI Support. 6.

**Interrupt** handling. **Interrupt handler** and. Bottom half/tasklet threads ...

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**Interrupt handler** replies to acknowledge **interrupt**.  $\phi$ . IRQ gets re-enabled on PIC ...

**Hints** for easy start.  $\phi$ . Simple read/write interface ...

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ister (although the compiler is free to ignore the **hint**), and you will not be taking the address of ... are not needed in an **interrupt handler** or something ...

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tion of the **interrupt handler**. (c) Describe the hardware needed to speculate load-store dependencies (**hint**: this is required to ...

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—i.e. an **interrupt handler** being interrupted ... Higher priority lines can **interrupt** lower priority ... **Hint**: how much are the system buses. available? ...

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**[PDF]** Lecture 15: Monitors and Processes in Mesa

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General Principle: use **hints** for performance that have little or better ... Interrupts:

**interrupt handler** can't afford to wait to acquire a monitor lock. ...

db.cs.berkeley.edu/cs262/2005/lecs/mesa.pdf - [Similar pages](#)

**[PDF]** Introduction to Linux Device Drivers

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to be called directly from the timer **interrupt handler**. It also creates two functions: ...

**Hint**: can tasklets block? Last, it releases the lock. ...

www.mulix.org/lectures/intro\_to\_linux\_device\_drivers/intro\_linux\_device\_drivers.pdf - [Similar pages](#)

**[PDF]** L4Ka::Pistachio PowerPC Implementation

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Unmasking the **interrupt** vector after the **interrupt handler** processes the ... epilog code, and thus the noreturn **hint** requires explicit support in the archi- ...

l4ka.org/projects/pistachio/powerpc/ppc.pdf - [Similar pages](#)

**[PDF]** Towards Scalable Multiprocessor Virtual Machines

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within a low-level **interrupt handler**). To conclude, we see that spin-locks are and will be ... **hints** to the virtual machine layer (intrusive), or have the ...

l4ka.org/publications/2004/

Towards-Scalable-Multiprocessor-Virtual-Machines-VM04.pdf - [Similar pages](#)

**[PDF] SMIPS Processor Specification**

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**interrupt handler** running in kernel mode with further interrupts disabled. ... except no **trap** is created on overflow. SLT and SLTU performed signed and ...  
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**[PDF] SMIPS Processor Specification**

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trapped and can be emulated in software by a **trap handler**. ... ExcCode Mnemonic Description. 0 **Hint**. External **interrupt**. 2 Tint. Timer **interrupt**. ...  
[www.csg.lcs.mit.edu/6.884/handouts/labs/smips-spec.pdf](http://www.csg.lcs.mit.edu/6.884/handouts/labs/smips-spec.pdf) - [Similar pages](#)

**[PDF] Concurrent Garbage Collection Using Hardware-Assisted Profiling**

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instructions and **hint** bits, and pipeline tuning features that are ... or it is retired, ProfileMe generates an **interrupt**, and a **trap handler** ...  
[www.ece.wisc.edu/~jes/papers/ismm00.heil.pdf](http://www.ece.wisc.edu/~jes/papers/ismm00.heil.pdf) - [Similar pages](#)

**[PDF] Rotary Encoder for 16LX-Series**

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**Hint 2:** some **Interrupt**-sources will use the same the **Interrupt-Handler**, like INT0 and INT1. This makes additional software necessary within the ...  
[apps.fmg.de/.../appnotes/Public/16Bit/mcu-an-390055-e-rotary\\_encoder/mcu-an-390055-e-v12-rotary\\_encoder.pdf](http://apps.fmg.de/.../appnotes/Public/16Bit/mcu-an-390055-e-rotary_encoder/mcu-an-390055-e-v12-rotary_encoder.pdf) - [Similar pages](#)

**[PDF] Midterm I SOLUTIONS**

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1) The user program can execute a **trap** instruction (for a system call) ... appropriate **interrupt handler**. The function of the **interrupt** controller is to ...  
[hkn.eecs.berkeley.edu/student/online/cs/162/2005/fa-1-sol.pdf](http://hkn.eecs.berkeley.edu/student/online/cs/162/2005/fa-1-sol.pdf) - [Similar pages](#)

**[PDF] CS 354 Final Exam, 33 1/3% Monday, December 18th, 2000 Solution**

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**Hint:** Show the equation to calculate the new speedup. ... The keyboard **interrupt handler** was responsible for recognizing if a key had been pressed. ...  
[www.cs.wisc.edu/~cs354-1/exams/E3.dd.f00.pdf](http://www.cs.wisc.edu/~cs354-1/exams/E3.dd.f00.pdf) - [Similar pages](#)

**[PDF] White Paper: Ubicom IP3023 Wireless Network Processor**

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IP3023 processor can start executing that **interrupt handler** on the very next cycle. ... one-bit **hint** to suggest that a branch will jump forward or backward. ...  
[www.ubicom.com/pdfs/whitepapers/WP-IP3023WNP-01.pdf](http://www.ubicom.com/pdfs/whitepapers/WP-IP3023WNP-01.pdf) - [Similar pages](#)

**[PDF] Introduction to Linux Device Drivers**

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called directly from the timer **interrupt handler**. It also. creates two functions, register\_timer\_interrupt and ... never do here? **hint:** can tasklets block?) ...  
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**[PDF] Linux Kernel Debugging**

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dump core in an **interrupt handler** and no oops. data makes it to disk - you drop into the debugger ... sometimes it's no more than a general **hint** to ...  
[www.haifux.org/lectures/63/kernel\\_oopsing.pdf](http://www.haifux.org/lectures/63/kernel_oopsing.pdf) - [Similar pages](#)

**[PDF] Evaluating the Performance Overhead of Object-Oriented Techniques ...**

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serves as a **hint** to the compiler, this is the best that we can. achieve while still retaining a ... in the **interrupt handler** itself, DARK++ uses a minimal ...  
web-cat.cs.vt.edu/PEBB/R070\_S\_Bhaktavatsalam.pdf - [Similar pages](#)

**[PDF] SRC 166**

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At each profiling **interrupt**, the driver reverts the user-. mode context to the library's user-mode **trap handler** that runs the interpreter, logs ...  
www.hpl.hp.com/techreports/Compaq-DEC/SRC-RR-166.pdf - [Similar pages](#)

**[PDF] CS 110 Practice Final Examination 2**

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**Hint:** the table on page 1 might prove useful. Instruction. Next PC (32-bit) ... Assuming that the UART is set up, write the **interrupt handler** for receive: ...  
www.stanford.edu/class/cs110/handouts/37\_Practice\_Final\_2.pdf - [Similar pages](#)

**[PDF] TMS320VC5471/TMS320VC5470 Inter-Processor Communication**

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api\_handler() in the same file is the dedicated **interrupt handler** for the API **interrupt**. ... To **interrupt** the ARM, the DSP pulses BSCR[3] (**HINT**). ...  
focus.ti.com/lit/an/spra818/spra818.pdf - [Similar pages](#)

**[PDF] CS4411 Spring 2006 HW 1 (Due: Feb 16th, 2006, in class)**

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**interrupt handler** for incoming messages in favor of other existing or future jobs in the victim. machine. Be as specific as you can (**Hint:** Split message ...  
www.csl.mtu.edu/cs4411.choi/www/Homework/hw106s.pdf - [Similar pages](#)

**[PDF] Diagnosing Kernel Problems**

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The first lines give a **hint** why the exception happened. In this case, this is an invalid ... is only possible if it is not an **interrupt handler** oops. ...  
suse.osuosl.org/people/rschmid/SLE10\_Transfer/l3-diagnosis-workshop.pdf - [Similar pages](#)

**[PDF] CPS 110 Problem Set #1**

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When a process enters the kernel via a system call **trap**, it becomes ... As an optimization, the receiver **interrupt handler** services reply messages ...  
www.cs.duke.edu/~chase/cps210-archive/cps110-probs.pdf - [Similar pages](#)

**[PDF] High-Speed Hardware/Software Co-Verification with CPU Model ...**

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Detects I/O access and **interrupt handler** in software code, and ... needs **hint**. Converter changes "accessing to user specified pointer" into store/load ...  
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**[PDF] High-Speed Hardware/Software Co-Verification with CPU Model ...**

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Detects I/O access and **interrupt handler** in software code, and. automatically converts them into method call of ... "I/O accessing with pointer" needs **hint** ...  
www.interdesigntech.co.jp/pdf/nascug.pdf - [Similar pages](#)

**[PDF] COMP 310: Operating Systems**

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Jump to **interrupt handler** (in kernel). . How does it find this? ... **interrupt**. . An **interrupt** in software is called a **trap** ...

home.sandiego.edu/~calvarado/COMP310/Lectures/COMP310\_Lecture25-2up.pdf -

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**[PDF] CS 416: Operating System Design**

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**Hints**:. 1. Write your name and student number on the exam book NOW! ... timer **interrupt handler**, because it would suspend the **interrupt handler** and not the ...  
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**[PDF] Exceptions in MIPS**

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that the **interrupt handler** can use these registers without having to save them ...

Begin by making a copy of the file called **trap.handler**: call the copy ...

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**[PDF] Microsoft PowerPoint - 07 Input Output.ppt**

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—i.e. an **interrupt handler** being interrupted ... on DMA? • What about on board cache? • **Hint**: how much are the system buses. available? ...

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**[PDF] Upcoming Event Updates from HI-TECH Software**

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**Hint**: Timer 2 has a period comparison facility. With reload. value = F9h; prescaler = 1:16 and ... **interrupt handler** for the timer so that it toggles the ...

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**[PDF] T : A Software Framework for Component-based Operating System Kernels**

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dress space model, **interrupt** handling model, or commu- nication model). ... syscall **trap handler** then calls the target interface com- ponent. ...

www.diku.dk/~julia/Think.pdf - [Similar pages](#)

**[PDF] Processor Scheduling**

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has an additional thread parameter that gives a hint to the scheduler that scheduling ... range check of the instruction pointer in the **interrupt handler**. ...

www.opus.ub.uni-erlangen.de/opus/

volltexte/2004/37/pdf/07\_Processor\_Scheduling.pdf - [Similar pages](#)

**[PDF] (7%) in > > D. I), B in in**

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**Hint**: Use a 3-bit shift register. 3. (10%) Design a vector-**interrupt** ... subsystem, device driver, **interrupt handler**, until device controller and back, ...

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allocator and the **trap handler**. This section first describes the data ... appl hint() .

When an application. program calls this routine and there is an ...

[cs.ubc.ca/rr/proceedings/spe91-95/spe/vol23/issue10/spe852.pdf](http://cs.ubc.ca/rr/proceedings/spe91-95/spe/vol23/issue10/spe852.pdf) - [Similar pages](#)

**[PDF] Linux Kernel Synchronization**

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One **interrupt handler** for different IRQs share data within it; the **interrupt handler** might be reentrant ... (hint: the purpose of `smp_rmb()` and `smp_wmb()`) ...

[www.cs.ccu.edu.tw/~lhr89/linux-kernel/Linux%20Kernel%20Synchronization.pdf](http://www.cs.ccu.edu.tw/~lhr89/linux-kernel/Linux%20Kernel%20Synchronization.pdf) -

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**[PDF] Question Score 1 2 3 Total**

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(Hint: this voltage is caused. by a change in current through an inductor). ... (d) Write the ritual and the **interrupt handler** for the slave.

[www.async.ece.utah.edu/~myers/ece3720/handouts/midterm2.pdf](http://www.async.ece.utah.edu/~myers/ece3720/handouts/midterm2.pdf) - [Similar pages](#)

**[PDF] IBM XL C/C++ Compilers for Mac OS X**

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Hints and tips to improve portability with Mac OS X ... exception format, `format_arg`, `function_vector`, **interrupt**, **interrupt handler**, ...

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**[PDF] Network Working Group SNMPv2 Working Group**

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type "SNMP **Trap Handler**" (which consists of seventeen ASCII. characters). ... a hint to perform an NBP confirm (which sends a unicast to the ...

[portal.etsi.org/docbox/Reference/IETF/RFC/RFC1906.pdf](http://portal.etsi.org/docbox/Reference/IETF/RFC/RFC1906.pdf) - [Similar pages](#)

**[PDF] Project 3: Writing a Kernel From Scratch**

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enumerate the situations in which it might be invoked (hint: not just by the timer **interrupt. handler**). Before a thread runs for the first time, ...

[www.cs.cmu.edu/~410-s04/p3/kernel.pdf](http://www.cs.cmu.edu/~410-s04/p3/kernel.pdf) - [Similar pages](#)

**[PDF] Linux Kernel Hacking Free Course**

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Hint: using `smp_affinity()` to bind irq lines to specific processors. Hint: using `smp_affinity()` to bind irq ... by jumping to the proper **interrupt handler** ...

[bravo.ce.uniroma2.it/kernelhacking2006/lkh06\\_11b\\_s.pdf](http://bravo.ce.uniroma2.it/kernelhacking2006/lkh06_11b_s.pdf) - [Similar pages](#)

**[PDF] CS 540 - Operating Systems - Final Exam - Name: Date: Monday, May ...**

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(A) **Interrupt handler** (B) **Interrupt vector** (C) **Interrupt indicator** (D) **Interrupt signal** ... (Hint: Be careful and draw a picture.) (10 points) ...

[www.cs.wichita.edu/~chang/lecture/cs540/exam/final-03.pdf](http://www.cs.wichita.edu/~chang/lecture/cs540/exam/final-03.pdf) - [Similar pages](#)

**[PDF] EP414 Instrumentation Design Laboratory Manual**

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6.3 Hints. The prototype for an RTEMS **interrupt handler** is: `rtems_isr interruptHandler (rtems_vector_number v);`. The following code attaches the MC68360

...

[engrwww.usask.ca/classes/EP/414/lab/ep414labmanual/labmanual.pdf](http://engrwww.usask.ca/classes/EP/414/lab/ep414labmanual/labmanual.pdf) -

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**[PDF] XFI: Software Guards for System Address Spaces**

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a kernel **interrupt handler**), XFI could bound the length. of execution before a support routine ... and verification **hints**, and use the allocation stack for ...  
[research.microsoft.com/research/sv/gleipnir/xfi.pdf](http://research.microsoft.com/research/sv/gleipnir/xfi.pdf) - [Similar pages](#)

**[PDF] Experience with Processes and Monitors in Mesa**

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instructions, or through a **trap** vector in the case of fault queues. ... **interrupt handler** processes is created to match the actual hardware configuration, ...  
[research.microsoft.com/~blampson/23-ProcessesInMesa/Acrobat.pdf](http://research.microsoft.com/~blampson/23-ProcessesInMesa/Acrobat.pdf) - [Similar pages](#)  
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**[PDF] Laboratory assignments:**

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To connect an **interrupt handler** with its. **interrupt** vector, the routine ... 5.2 Practical **hints**. You should structure the problem by drawing an access graph ...  
[www.ce.chalmers.se/edu/course/EDA222/Documents/Literature/lab2\\_pm\\_06\\_eng.pdf](http://www.ce.chalmers.se/edu/course/EDA222/Documents/Literature/lab2_pm_06_eng.pdf)  
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**[PDF] T U B C D E C E EECE 379 : Design of Digital and Microcomputer ...**

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**Hint:** If the required specification is not given, use two specifications ... (b) The keyboard **interrupt handler** in a PC is located at absolute memory ...  
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**[PDF] Project 3: Precise Interrupts (15%)**

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**handler.** Hardware loads this right before vectoring to an exception, **interrupt**, or. **trap handler.** The first thing that a **handler** should do is save this ...  
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**[PDF] Project 3: Precise Interrupts (15%)**

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Hardware loads this right before vectoring to an exception, **interrupt**, or **trap handler**. The. first thing that a **handler** should do is save this value in a ...  
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Compiler **Hints** and Tips. Compiler optimisation options • Writing efficient code ... Development of drivers, **interrupt handler**... ARM SoC Design (4 or 5-day) ...  
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**[PDF] Scheduling Support for Concurrency and Parallelism in the Mach ...**

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The clock **interrupt handler** performs this check for running threads, ... can use a scheduling **hint** to encourage the operating system to run the target. ...  
[lass.cs.umass.edu/~shenoy/courses/spring02/readings/black90scheduling.pdf](http://lass.cs.umass.edu/~shenoy/courses/spring02/readings/black90scheduling.pdf) - [Similar pages](#)

**[PDF] Proceedings of the 2001 USENIX Annual Technical Conference**

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nished with a switch **hint**. This **hint** overrides the sys-. tem's standard policy of scheduling ... the lateness of a user-level **interrupt handler**. Second, we ...  
[usenix.org/events/usernix01/full\\_papers/hohmuth/hohmuth.pdf](http://usenix.org/events/usernix01/full_papers/hohmuth/hohmuth.pdf) - [Similar pages](#)

**[PDF] Microsoft PowerPoint - Chapter06.ppt**

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**Hint:** what happens if one kernel procedure calls another? Kernel Exit & Entry ... needs to be examined by the **interrupt handler** on each clock tick. ...  
[www.homes.doc.ic.ac.uk/~xf1/teaching/operating-systems/Chapter06-4up.pdf](http://www.homes.doc.ic.ac.uk/~xf1/teaching/operating-systems/Chapter06-4up.pdf) - [Similar pages](#)

**[PDF] Collecting and Exploiting Cache-Reuse Metrics**

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reuse metrics which are supposed to give more precise **hints** on how ... **interrupt handler** which is triggered at overflow time of a hardware performance ...  
[www.bode.in.tum.de/~weidendo/publications/iccs05.pdf](http://www.bode.in.tum.de/~weidendo/publications/iccs05.pdf) - [Similar pages](#)

**[PDF] On RAMSES Version 3.0**

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internet, and other **hints**. All this documentation should help you to make good ... **interrupt handler** actually sits in the hard disk driver and can therefore ...  
[www.sysecol.ethz.ch/RAMSES/Documents/On\\_RAMSES\\_READ\\_ME.pdf](http://www.sysecol.ethz.ch/RAMSES/Documents/On_RAMSES_READ_ME.pdf) - [Similar pages](#)

**[PDF] Pragmatic nonblocking synchronization for real-time systems 1 ...**

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nished with a switch **hint**. This **hint** overrides the system's standard policy of scheduling the threads, ... level **interrupt handler**. Second, we measured the ...  
[os.inf.tu-dresden.de/~hohmuth/prj/usenix2001.pdf](http://os.inf.tu-dresden.de/~hohmuth/prj/usenix2001.pdf) - [Similar pages](#)

**[PDF] THE BCS PROFESSIONAL EXAMINATION Certificate October 2003 ...**

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**HINT:** What addressing mode is made use of during the evaluation of this expression? ... b) A particular computer takes 5  $\mu$ s to call an **interrupt handler** in ...  
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**[PDF] Using Polled or Interrupt-driven Timers**

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This document will also provide **hints** and a useful ... While you are inside the **interrupt handler** every other operation is on hold. Therefore the only ...  
[www.ifrobotics.com/docs/timers\\_white\\_paper\\_2004-jan-14.pdf](http://www.ifrobotics.com/docs/timers_white_paper_2004-jan-14.pdf) - [Similar pages](#)

**[PDF] EE3376 – Embedded Systems - Spring 2004 - Exam 2 – MacDonald – Page 1**

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instruction executed in the **interrupt handler** subroutine. ... **Hint:** Chapter 5 of the Valvano book includes details about the Timer for the HC12 ...  
[www.ece.utep.edu/courses/web3376/homework/ee3376\\_exam2\\_solutions.pdf](http://www.ece.utep.edu/courses/web3376/homework/ee3376_exam2_solutions.pdf) - [Similar pages](#)

**[PDF] Thread/Synchronization Exercises**

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preempted in favor of a higher priority thread or **interrupt handler** in the CPU, ... **Hint:** Consider what could happen to nodes that are freed once they ...  
[www.i.u-tokyo.ac.jp/edu/training/ss/lecture/new-documents/Projects/ThreadExercises.pdf](http://www.i.u-tokyo.ac.jp/edu/training/ss/lecture/new-documents/Projects/ThreadExercises.pdf) - [Similar pages](#)

**[PDF] CISH-4030 Structured Computer Architecture Input/Output Problems**

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Check for **interrupt** at end of each instruction cycle ... i.e. an **interrupt handler** being

interrupted ... **Hint:** how much are the system buses available? ...

[www.rh.edu/~rhb/sca/sca07.pdf](http://www.rh.edu/~rhb/sca/sca07.pdf) - [Similar pages](#)

**[PDF]** [Department of Computer Science](#)

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**Hints:** Do NOT write this in assembly language nor in your favourite ... **INTERRUPT**

**HANDLER.** ToD: data # datum holding the current date and time in ticks ...

[www.cs.ucl.ac.uk/staff/S.Wilbur/1b11/1b11%20cw02.pdf](http://www.cs.ucl.ac.uk/staff/S.Wilbur/1b11/1b11%20cw02.pdf) - [Similar pages](#)

**[PDF]** [Extra Review Questions](#)

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(**Hint:** your machine should be very similar to the one in a). ... **interrupt** occurs. a)

What does the timer **interrupt handler** do? ...

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mouse\_handler - the low level **interrupt handler** calls this \*/ ... (**Hint:** Get into graphics mode for better results). Suggested Projects ...

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**[PDF]** [Abstract 1 Introduction](#)

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Client code must still use GASNet no-**interrupt** sections and **handler-safe** ... GASNet is free to ignore the value of the **hint** and choose a different segment ...

[gasnet.cs.berkeley.edu/258-paper.pdf](http://gasnet.cs.berkeley.edu/258-paper.pdf) - [Similar pages](#)

**[PDF]** [Goals Requirements Preparation Background](#)

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(**Hints:** if you used the suggested address range for the core, the default reset address, ... exception **handler**. 5. **interrupt handler**. 6. program clean ...

[www.eecg.toronto.edu/~pc/courses/edk/modules/6.2/m05.pdf](http://www.eecg.toronto.edu/~pc/courses/edk/modules/6.2/m05.pdf) - [Similar pages](#)

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(trap OR interrupt) handler hint file [Search](#)

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**interrupt** vector that is used by the HW **break** mechanism. ... will **break** both fetch from memory and fetch from the CPU internal **prefetch**. register. ...  
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To view **interrupt** default **handler** initialization, see Figure 2 on page 9. ...  
Abort-status stack must be initialized for Data and **Prefetch** Abort handling. ...  
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Because there are no data caches, it is unnecessary to block, **prefetch**, worry ... The **break** instruction is left in place; a special breakpoint **trap handler** ...  
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**Interrupt Handler** with **Prefetch**. Handle Finish. Handle Miss. Handle Access.  
Miss-based. Prediction ... ioctl(fd, VMW\_IOC\_RESUME, &params); **break**; ...  
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**interrupt** IPL, **interrupt** enable or **interrupt** flag may. cause an address error **trap**. ...  
**trap handler** routine prior to exiting the **trap handler** ...  
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Sequential MAC class instructions, which **prefetch** ... of events will lead to an address error **trap**. The ... can be read in the QE1 **interrupt handler** and ...  
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**interrupt handler**, the NI can cause a running user-level process to asynchronously ... to **prefetch** message data from local memory into the message buffer if ...  
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Using an **interrupt handler** or using a separate thread running in the kernel. ...  
Increasing the cache line size results in very effective **prefetch**- ...  
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When the processor takes an **interrupt** or **prefetch** abort the ETM will sometimes ... continued when the **interrupt handler** exited. [DE 34137] ...

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As with ARMulator, the ARM debuggers provide **break**, watch, unbreak, and ... In the case of a system with no **interrupt handler** that has an active source of ...

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The processor's Data **Prefetch** Logic speculatively fetches ... cycle, the interrupter issues the ID to the **interrupt handler**. ...

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0x00000004. Software **Interrupt** (SWI). SVC. 0x00000008. **Prefetch** abort ... ;Timer0 **interrupt**. IMPORT IRQC\_Timer0. IRQASMTimer0 **HANDLER** IRQC\_Timer0 ...

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**prefetch** logic speculatively fetches data to the L2 cache before an L1 ... **Interrupt Handler**: The **interrupt handler** monitors, and can be ...

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processor's data **prefetch** logic speculatively fetches data to the ... **Interrupt Handler**: The **interrupt handler** monitors, and can be ...

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executed starting in the **trap handler** (and beyond) af- ... to convert the load into a **prefetch**, since prefetches can. retire before their misses complete. ...

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we need to **prefetch** three nodes ahead to hide the entire miss la- tency. Therefore, we would want to ... Second, a user-level **trap handler** could be used ...

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The **trap handler** can handle simple exceptions; others are handled by the ... or backward, it can **prefetch** data into the cache before the next request is ...

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to **break** into an executing thread and to call a procedure. The **interrupt** ... The **trap handler** can handle simple exceptions; others are handled by the ...

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level) exception **handler** for **trap #1** must be installed at address 0x84. ... environment  
we install an **interrupt handler** for the serial interface. ...  
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&Xint0x80\_syscall, which is the address of the **interrupt handler**. The third parameter  
is the constant SDT\_SYS386TGT, which means that this gate is. a **trap** ...  
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sponding **interrupt handler** or, (ii) using a separate thread ... Increasing the cache  
line size results in effective **prefetch**- ...  
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**trap** instruction jumps to **trap handler**. hardware saves PC in IAR. **trap handler** must  
save IAR ... **interrupt** may occur in order different from sequential CPU ...  
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Based on code inspection, here is a **break down** ... path and **interrupt handler** across  
CPUs to nar- ... termine how early one can **prefetch** that data. ...  
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Consequently, an **interrupt handler** may either load. words directly from this array via  
the ... Software **prefetch** is implemented in Alewife as two different ...  
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for dispatching rapidly to the appropriate **trap handler**. ... (Sparcle and its memory  
controller provide non-binding **prefetch** instructions aswell.) ...  
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Consequently, an **interrupt handler** may. either load words directly from this array via  
the ... different colored load instructions, one for read **prefetch** ...  
[www.cs.berkeley.edu/~kubitron/papers/alewife/pdf/alewife-ieee.pdf](http://www.cs.berkeley.edu/~kubitron/papers/alewife/pdf/alewife-ieee.pdf) - [Similar pages](#)  
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They propose a tagged store buffer and **prefetch** ... Append In-line scheme: In-line  
the **interrupt handler** by fetching the instructions at the tail of the ...  
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9. **Prefetch Abort Handler**. 26. 10. Data Abort **Handler** ...

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the programmer to **prefetch** when anticipating a cache miss. ... The **interrupt handler** reads the status registers to find out what caused interrupts (this ... [kernel.org/pub/linux/kernel/people/hadi/docs/UKUUG2005.pdf](http://kernel.org/pub/linux/kernel/people/hadi/docs/UKUUG2005.pdf) - [Similar pages](#)

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on a miss, it fetches a whole block, hence we get a kind of **prefetch** of the rest of the ... defined **interrupt handler** called `zzexternal_interrupt`. ... [www.idt.mdh.se/utbildning/exjobb/files/TR0094.pdf](http://www.idt.mdh.se/utbildning/exjobb/files/TR0094.pdf) - [Similar pages](#)

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This is the **Prefetch Abort interrupt handler** ... `break; case 0x14: /* Reserved - should never happen */. break; case 0x18: /* IRQ */ ...` [www.intel.com/design/iio/aplnots/27343803.pdf](http://www.intel.com/design/iio/aplnots/27343803.pdf) - [Similar pages](#)

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When this happens, the **prefetch abort handler** can usually safely ... **interrupt handler** had not yet seen that flag and serviced it. ... [www.intel.com/design/iio/specupdt/27341511.pdf](http://www.intel.com/design/iio/specupdt/27341511.pdf) - [Similar pages](#)  
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for dispatching rapidly to the appropriate **trap handler**. ... Sparcle and its memory controller provide non-binding **prefetch** instructions aswell. ... [www.ee.umd.edu/~yeung/papers/sparcle.pdf](http://www.ee.umd.edu/~yeung/papers/sparcle.pdf) - [Similar pages](#)

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the instrumentation code or data collected may inadvertently **break** ... the start of an **interrupt handler**, and it reaching another location, ... [compilers.cs.ucla.edu/emsoft05/TitzerPalsberg05.pdf](http://compilers.cs.ucla.edu/emsoft05/TitzerPalsberg05.pdf) - [Similar pages](#)

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... DL=Drive, ES:BX=Ptr to buffer. • Now let's take a look at the Stoned **interrupt handler**... ... **Prefetch-queue** attack, eg., make code work correct only when ... [www.engsci.aau.dk/~bia/F06/Sap/SAP-3.pdf](http://www.engsci.aau.dk/~bia/F06/Sap/SAP-3.pdf) - [Similar pages](#)

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translation does not exist for the **interrupt handler** at real. PowerPC. address ... when a cache miss occurs, or data from a prior **prefetch** is ... [www.cis.upenn.edu/~cis700-6/04f/papers/ebcioglu-bin-trans.pdf](http://www.cis.upenn.edu/~cis700-6/04f/papers/ebcioglu-bin-trans.pdf) - [Similar pages](#)

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caches, a small (2-KB) L2 cache and **prefetch** buffer, and. 4 MB of embedded dynamic random access ... from an **interrupt handler**. The torus (and collective) ... [www-fp.mcs.anl.gov/~toonon/Papers/mpi-bgl-ijrd-2005.pdf](http://www-fp.mcs.anl.gov/~toonon/Papers/mpi-bgl-ijrd-2005.pdf) - [Similar pages](#)

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is that **interrupt** latencies are unknown, since an inter- ... a **BREAK** operation. The debug exception **handler** may. implement a count mechanism in software, ... [www.springerlink.com/index/U6T11N176862P03K.pdf](http://www.springerlink.com/index/U6T11N176862P03K.pdf) - [Similar pages](#)

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way, the initial cache miss of a reference stream invokes the appropriate **trap handler**, which, in. turn, allocates a **prefetch** engine and initiates ... [www.arctic.umn.edu/papers/svw-phd-thesis-98.pdf](http://www.arctic.umn.edu/papers/svw-phd-thesis-98.pdf) - [Similar pages](#)

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BKPT instruction to **trap** at breakpoints. Execution of. this instruction causes the processor to be interrupted. with a **Prefetch Abort interrupt**. ... [choices.cs.uiuc.edu/choices-arm.pdf](http://choices.cs.uiuc.edu/choices-arm.pdf) - [Similar pages](#)

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First instruction in decremter or external **interrupt handler** may be ... The branch remains unresolved long enough for a **prefetch** of the first cache line ... [www.freescale.com/files/32bit/doc/errata/MPC860CE.pdf](http://www.freescale.com/files/32bit/doc/errata/MPC860CE.pdf) - [Similar pages](#)  
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abort protocol is used by an exokernel to **break** secure bindings of ... saving and restoring all caller-saved registers when a **trap handler** ... [pdos.csail.mit.edu/6.828/2006/readings/engler95exokernel.pdf](http://pdos.csail.mit.edu/6.828/2006/readings/engler95exokernel.pdf) - [Similar pages](#)

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Implication: PREFETCHH instructions may not perform the data **prefetch** if ... stack has the AC flag set, and the **interrupt handler's** stack is misaligned. ... [download.intel.com/design/mobile/SPECUPDT/31407905.pdf](http://download.intel.com/design/mobile/SPECUPDT/31407905.pdf) - [Similar pages](#)

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When enabling **prefetch** to the area set to the Little endian, ... event **break**. **Interrupt handler** to NMI request (tool) ... Coprocessor absent **trap** ...

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Usually a protocol over the SIPIO registers within the **interrupt handler** informs ... send out instruction physical address to start **prefetch** of cache line. ...

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`request_irq()` registers your hardware **interrupt handler** ... for core code and infrastructure then drivers and other code which doesn't **break** anything ...

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**interrupt handler**. Hence, it looks only at PowerPC archi- tected registers. ... a cache miss occurs or data from a prior **prefetch** is not yet. available. ...

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**interrupt handler** for storage exceptions. If a translation does not exist for ... cache CPI penalty using a history-based **prefetch** mechanism. ...

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of a high performance **interrupt** architecture subsystem; other topologies are ... **handler** needs to branch directly to the appropriate **trap handler** instead of ...

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Suppose that **interrupt A** occurs with. **handler X**, then **interrupt B** occurs with. **handler Y**. ... boundary, "**prefetch**" the next page in case the. CPU needs it. ...

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save its context: each subsequent timer **interrupt** (which demarcates ... saving and restoring all caller-saved registers when a **trap handler** ...

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**prefetch** sequential instructions and perform branch prediction to keep ...

**interrupt-intensive** applications can partition exception **handler** code into ...

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**break** points. detecting, 227. removing, 233. stopping, 454 ... for **interrupt handler**, 218. in kernel mode. See kernels, memory. scanning. paging, 515-517 ...  
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PEBS **interrupt handler** 1415. PEBS **interrupt** threshold 1368. PEBS Record Format 1370. PEBS, enabling 1415. PEN# 504. Pending **Break Event** 1316. Pentium 820 ...  
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Third, by using an abort protocol, an exokernel can **break** ... saving and restoring all caller-saved registers when a **trap handler**. starts and returns. ...  
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two **prefetch** buffers one to **prefetch** code in a linear ... vector to an **interrupt handler** after the current instruction execution is completed ...  
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For example, the **interrupt handler** should never do anything like: ... For example, a **Prefetch Abort** exception located at address ...  
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For example, a **Prefetch Abort** exception located at address ... Listing 8(8) The spurious **interrupt handler** does not nest, because it never unlocks ...  
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Identifying an **interrupt handler** is done by using one of ... tion **prefetch** queue. This mechanism enables the overlap of instruction decoding, instruc- ...  
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**Trap handler**. UltraBridge. Processor Interconnect interface. CPU. Generic CPU ... the store buffer, **prefetch** cache and write cache by commenting out the ...  
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As with all forms **trap-driven** simulation, a **trap handler** for write-back simulation must ... For example, a memory system can **prefetch** instructions or data ...  
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knowledge while MIPS Topsy needs acknowledgement to **break** repetitions, see ... call **trap handler** \*. \* Define the **Interrupt Handlers**.\* ...  
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It flushes the 16bit instructions from the instruction **prefetch** pipe by jumping ... kernel's **interrupt handler**. The **handler** finds out the source of ...  
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register indicates the PCI **interrupt** pin PIRQA# is used for routing Serial ... I/O instruction to ensure that the I/O **trap SMI handler** will be called before ...  
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Using the non-**prefetch** registers to initiate read transactions on the PCI bus of the A0-step ... **Interrupt handler** determines there is a timer **interrupt**. ...  
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with its 16-word **prefetch** buffer eventually may have re- duced execution time during measurements in a ... Here, the **interrupt handler** on the host imme- ...  
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L4 installs an internal **interrupt handler** for each line, that ... In the PII and PIII processors, certain **prefetch** operations are in- ...  
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instruction **prefetch** mechanism during idle bus activity ... the **interrupt handler**, and makes patches to the system needed by the driver. The open ...  
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device **interrupt handler** recieves the packet and puts it into a recieve queue. ... we **prefetch** information associated with all the functions in the call ...  
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counter to the first instruction in the corrensponding **trap handler** and to update other. architectural state that are affected when an **interrupt** occurs. ...  
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by interposing itself at the **interrupt handler** routine entry points. The RTLinux ... The entry that handles **prefetch** aborts deals with faults when fetching ...  
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It causes a context switch to the **interrupt handler** similarly to a. hardware **interrupt** ... CDRAM can **prefetch** data from DRAM into SRAM buffer ...  
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illegal access by the operating system's **interrupt handler**. ... The adversary can **prefetch** memory location i into cache location j: ...  
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of flexibility to cache, gather, reorder, or **prefetch**, as methods ... rupts until the **interrupt handler** has had a chance to safely ...  
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single instruction **prefetch** buffer to eliminate stalls after data transaction ... SCI **interrupt handler** is NOT always the highest priority **interrupt** ...  
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**interrupt**, NMI, or reset condition causes the CPU to exit. this mode and resume normal operation. ... Software Debug **Break Point**. **Trap** to SW Debug **Handler** ...  
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Since some instructions manipulate the PS register earlier, the following exceptions may cause the **interrupt handler** to **break** or the PS flag to update its ...  
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an instruction **prefetch** buffer that reduces the impact of such ... MicroBlaze allows exception and **interrupt handler** routines to be located at any address ...  
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MicroBlaze can be configured to **trap** the following internal error ... MicroBlaze allows exception and **interrupt handler** routines to be located at any ...  
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to quickly **trap** upon cache misses to a miss **handler** which performs ... load to a **prefetch** is acceptable because we do not care about the result of the ...  
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register is saved in the "interrupt save area," the exception program ... saving and restoring all caller-saved registers when a **trap handler** ...  
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**interrupt**, at which time an **interrupt handler** can read the saved ... of these sequences and **prefetch** the rest of the stream when they are detected. ...  
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issued, the prefetching MSHR for the **prefetch** will keep. the virtual address and the push ... stedt and Dubois use a **trap handler** to trigger prefetching ...  
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**Prefetch** instructions for utilizing temporal locality. CS252, Lecture 15: Multimedia Instruction ... Only if it causes an exception or the **interrupt handler** ...  
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Install a **trap handler** that simply returns without handling the exception. ... target instructions as the target processor's instruction **prefetch**, typi- ...  
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as a **trap**). Usage:. The **interrupt** vector custom instruction is used exclusively by the exception **handler**. Instruction Type:. R. Instruction Fields: ...  
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breakpoints/watchpoints to cause debug **interrupt** service routines (ISR) to be activated ... the EmbeddedICE-RT logic in the processor generates a **Prefetch** ...  
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or Thumb state, a FIQ **handler** should leave the. **interrupt** by executing. SUBS PC,R14\_fiq,#4 ... parity error, frame error and **break** condition, each of ...  
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GPS Data Event **Handler**. Application Timer Event **Handler** ... Performance breakdown demonstrates operation (**prefetch**/decay). accuracy: ...  
[www.artist-embedded.org/docs/Events/2005/IST-NSF/Friday/IST-NSF\\_Princeton\\_MargaretMartonosi.pdf](http://www.artist-embedded.org/docs/Events/2005/IST-NSF/Friday/IST-NSF_Princeton_MargaretMartonosi.pdf) - [Similar pages](#)

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This option enables or disables the IDE **prefetch** mode. Pri mary Master P10 ...  
setvect(0x72,old\_handler); /\* Put back the old **interrupt handler** \*/ ...  
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exception **handler** does not operate correctly. When [TLB miss exception is ... Breaks address H'00001068 when the condition [**Prefetch** address **break** after ...  
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Breaks address H'00001068 when the condition [**Prefetch** address **break** after ... If an **interrupt** is generated at the program execution start or end, ...  
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Maskable **interrupt** immediately after STI instruction failure ... **prefetch** queue to the instruction cache occur simul- taneously, the instruction request ...

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or **interrupt**. Generally, PowerPC 620 polls the NIU by reading a ... The context switching is implemented by a short **trap handler** that saves the old program ...

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**trap handler** is invoked; it translates all of the per- ... Multiple **prefetch**. adaptive disk caching with strategic data. layout. ...

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(trap OR interrupt) handler prefetc

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